Remarks

In the office action, claims 1-36 were rejected. The Applicant has amended claims 1-11. No claims have been added or canceled. The amendments are supported by the originally filed specification and claims, and consequently, no new matter has been introduced. The Applicant respectfully requests reconsideration in light of the remarks to follow.

Rejections – 35 U.S.C. § 101

The Examiner rejected claims 1-10 under Section 101 because the claims were allegedly directed toward non-statutory subject matter. The Examiner asserted that a processing block comprising a plurality of sub-blocks are all software and/or software constructs. While the Applicant disagrees that a storage sub-block could be construed as software or a software construct, the Applicant has amended the claims to expedite allowance. The Applicant respectfully requests that the Examiner withdraw the rejection.

Rejection – 35 U.S.C. § 103(a)

Claims 1-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Motomura (US 5,815,727) ("Motomura"). The Applicant respectfully traverses the rejections.

Claim 1 currently recites:

> An apparatus comprising:
> a storage block configured to store a thread switching structure;
> an execution block configured to execute instructions; and
> a thread management block coupled to the storage and execution blocks, the thread management block equipped to store and maintain the thread switching structure in the storage block to facilitate interleaving execution of a plurality of threads of instructions by the execution block, with the thread switching structure including a current thread identifier identifying one of the plurality of threads as a current thread being currently executed by the execution block, and a thread array of thread entries, one per thread, correspondingly describing the plurality of threads, each thread entry being created and added to the thread array by the thread management block as part of the execution of a create thread instruction of a thread to spawn execution of another thread.

Claim 1 is directed toward an apparatus including a thread management block to store and maintain a thread switching structure that facilitates interleaving execution of a plurality of threads by the execution block. In other words, the same execution resource executes each of the

threads within the thread switching structure in an interleaved fashion. Motomura fails to teach or suggest such a recitation.

In contrast, Motomura teaches a general purpose parallel processing system where multiple processors are individually coupled to an ordered multithread executing system. The ordered multithread executing system manages the threads of a program and directs the various threads to multiple processors for parallel execution. As a consequence, Motomura expressly teaches away from utilizing a single execution resource (i.e., an execution block) to execute each of the threads within the thread switching structure. It is well known to those of ordinary skill, that given multiple parallel processors, execution of all threads on a single processor is to be avoided. Rather, it is desirable to have the instructions carried out concurrently across all processors. Therefore, when viewing the claim as a whole, as required by law, Motomura's parallel processing system fails to teach or fairly suggest an apparatus having an execution block to execute instructions provided from a thread switching structure maintained by a thread switching block. For at least this reason claim 1 is allowable over the cited art.

Claims 2-10 depend either directly or indirectly from independent claim 1, thereby incorporating its recitations. Therefore, for at least the same reasons that claim 1 is allowable, claims 2-10 are similarly allowable.

While allowable due to their dependence on allowable claim 1, claims 2-10 are further patentable over the cited reference. For example, claim 9 includes the recitation of an I/O interface configurable to be a selected one of an input interface and an output interface to particularize the apparatus as a selected one of an input processing block or an output processing block of a signal processing macroblock. This recitation clarifies that the single apparatus may be particularized and included in a signal processing macroblock to perform as either an input or output processing block. Motomura remains entirely silent with respect to a configurable I/O interface selectable to particularize the apparatus. Furthermore, it would not have been obvious to include such an interface within the processing system of Motomura. It is well known to those of ordinary skill in the art that a parallel processing system, such as the system of Motomura, would not be particularized as simply an input or output processing block of a signal processing macroblock. For at least this additional reason, claim 2 is allowable over the cited art.

Claim 11 includes recitations generally similar to those of independent claim 1. Therefore, for at least the same reasons that claim 1 is allowable over Motomura, claim 11 is similarly allowable.

Claims 12-17 depend either directly or indirectly from independent claim 11 thereby incorporating its recitations. Therefore, for at least the same reasons that claim 11 is allowable claims 12-17 are similarly allowable.

While allowable due to their dependence upon allowable claim 11, claims 12-17 are further patentable over the cited reference. For example, claims 13 and 15 include recitations relating to an activeness indicator of various thread entries in the thread array. The activeness indicators indicate whether a thread is in an active state and included in the threads to be executed or alternatively in an inactive state and excluded from the threads to be executed. The thread indicator may be reset from active to inactive by, for example a termination instruction of the thread being executed. In other words, while the thread is being executed and after its termination, there remains a corresponding thread entry in the thread array having an active or inactive status.

To teach or suggest this recitation, the Examiner relies on the virtual thread numbers of Motomura and threads in the waiting state as teaching inactive threads. The Applicants respectfully disagree with such an assertion. As the Examiner states, the threads of Motomura are ordered in the thread descriptor storage device according to a virtual thread number, and further, that threads in the waiting may receive a higher virtual thread number. The corresponding threads, however, are expressly included as threads to be executed. For example, Motomura expressly teaches the threads in the waiting state are among the threads to be executed (e.g. re-executed). *Motomura*, c.10 ll.39-41. If the threads are re-executed it is fundamental that they are included in the threads to be executed. Consequently, Motomura expressly teaches away from an activeness indicator indicating a thread is inactive and therefore not included among the threads to be executed, for example because the thread has terminated. Furthermore, those of ordinary skill in the art would readily understand Motomura as teaching a thread queuing mechanism for multiple processors. As each thread is removed from the queue, the remaining threads are renumbered accordingly until no threads are left and the processors may be shifted to a waiting state. Consequently, Motomura avoids the inclusion of threads

which are not to be processed, i.e. those threads which are inactive. For at least these reasons, the claims are further allowable.

Independent claim 18 includes recitations generally similar to those of independent claim 1, and is therefore, allowable for at least the same reasons. Claim 18, however, is further patentable over Motomura for additional reasons. For example, claim 18 includes as elements a selected one of an input processing block and an output processing block, wherein both include execution and thread management facilities and either an input or an output interface, respectively. Motomura, in contrast, teaches a general purpose parallel processor. It is well known to those of ordinary skill in the art to avoid utilizing a single processor of a multi-processor system as solely an input or output processing block. Consequently, when the instant claim is viewed as a whole, Motomura fails to teach or fairly suggest a processing block having dedicated execution and thread management facilities to function as either an input processing block or an output processing block. For at least this additional reason, claim 18 is allowable.

Claims 19-23 depend either directly or indirectly from independent claim 18 thereby incorporating its recitations. Therefore, for at least the same reasons that claim 18 is allowable, claims 19-23 are similarly allowable.

While allowable due to their dependence on allowable claim 18, claims 19-23 are further patentable over the cited reference. For example, claim 19 further defines the signal processing macroblock to include a computation block having execution and thread management facilities. Consequently, when viewing the claim as a whole, the claim includes either of an input or output processing block including its respective execution and thread management facilities, and additionally, a computation block including its execution and thread management facilities. In this manner, each of the blocks can function independently while interfacing with shared registers. Such recitations clearly demonstrate the ability to utilize the processing blocks as "building blocks" for a macroblock. Motomura, on the other hand, discloses multiple processors each sharing a single thread ordering system. Those of ordinary skill in the art will readily understand that the thread ordering system is required to interface with each processor to correctly order and distribute threads to the processors to ensure parallel processing and a sequential operation path for the threads. Consequently, Motomura expressly teaches away from individual processing blocks each including execution and thread management facilities.

Furthermore, Motomura fails to teach or fairly suggest the overall structure of utilizing various processing blocks to form a macroblock. For at least this additional reason claim 19 is allowable.

Claim 24 includes recitations generally similar to those of independent claim 1 and/or 18. Therefore, for at least the same reasons that claim 1 and/or 18 are allowable over Motomura, claim 24 is similarly allowable. For example, claim 24 includes the recitations of both an input and an output processing block including execution and thread management facilities. As discussed above, this architecture is neither taught nor suggested by the parallel processor system of Motomura. As stated previously, Motomura relies on a single thread ordering system to interface with the general purpose processors and provide the threads to the processors in a dedicated manner. Consequently, Motomura teaches away from devoting an independent thread ordering system to each of the processors. For at least this reason claim 24 is allowable over Motomura.

Claims 25-29 depend either directly or indirectly from independent claim 24 thereby incorporating its recitations. Therefore, for at least the same reasons that claim 24 is allowable, claims 25-29 are similarly allowable.

Additionally, claims 25-29 are further patentable over the Motomura. For example, claim 25 includes recitations similar to those discussed above with reference to claim 19. Claim 25, through its recitations, includes an input processing block, an output processing block, and a computation block, wherein each processing block includes execution and thread management facilities. As stated previously, Motomura's general purpose parallel processor teaches away from utilizing the various processors for specialized tasks, such as input, output, or computation; and further, dedicating execution and thread management facilities to each. Therefore, claim 25 is allowable for at least this additional reason.

Claim 30 includes recitations generally similar to those of independent claim 24. Therefore, for at least the same reasons that claim 24 is allowable, claim 30 is similarly allowable. Namely, claim 30 includes the recitations of both an input and output processing block as discussed at length above. Motomura fails to teach or fairly suggest the use of devoted processing blocks wherein each processing block includes execution and thread management facilities. For at least this reason claim 30 is allowable over Motomura.

Claims 31-36 depend either directly or indirectly from independent claim 30 thereby incorporating its recitations. Therefore, for at least the same reasons that claim 30 is allowable, claims 31-36 are similarly allowable.

While allowable due to their dependence on allowable claim 30, claims 31-36 are further patentable over Motomura. For example, claim 31 includes recitations generally similar to those discussed above with reference to claims 19 and 25. For at least this additional reason claim 31 is allowable over Motomura.

Conclusion

Claims 1-36 remain pending, no claims have been added or cancelled. As set forth above, Applicants submit that these claims are allowable and thus respectfully request their allowance. If the examiner has any questions regarding the substance of this office action response, he is invited to contact the undersigned at 503-796-2408.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,

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